AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently amended) An integrated circuit comprising a memory array having at least two planes ~~one plane~~ of memory cells formed above a substrate, said memory cells comprising thin film modifiable conductance switch devices and which cells are arranged in a plurality of series-connected NAND strings, said NAND strings including a series select device at each end thereof, wherein each respective NAND string within a given memory block of a given memory plane is coupled to a respective global bit line that is not shared by other NAND strings within the given memory block of the given memory plane, and wherein some adjacent NAND strings within a memory block are coupled at opposite ends thereof to their respective global bit lines.

2. (Canceled)

3. (Original) The integrated circuit of claim 1 wherein said switch devices include a charge storage dielectric.

4. (Original) The integrated circuit of claim 3 wherein said charge storage dielectric comprises an oxide-nitride-oxide dielectric stack.

5. (Original) The integrated circuit of claim 1 wherein said switch devices include a floating gate electrode.

6. (Currently amended) The integrated circuit of claim 1 wherein adjacent NAND strings are respectively coupled to a respective global bit line by way of a respective zia structure having a pitch matching that of the ~~adjacent~~ NAND strings.

7. (Canceled)

8. (Original) The integrated circuit of claim 1 further comprising NAND strings having an identical pitch as respective global bit lines associated therewith.

9. (Original) The integrated circuit of claim 1 wherein the memory cell devices and series selection devices forming each NAND string are structurally substantially identical.

10. (Currently amended) The integrated circuit of claim 1 ~~claim 2~~ wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

11. (Currently amended) The integrated circuit of claim 1 ~~claim 2~~ wherein the substrate comprises a polycrystalline substrate.

12. (Currently amended) The integrated circuit of claim 1 ~~claim 2~~ wherein the substrate comprises an insulating substrate.

13. (Original) The integrated circuit of claim 1 wherein the thin film modifiable conductance switch devices comprise silicon nanoparticles.

14. (Original) The integrated circuit of claim 1 wherein the thin film modifiable conductance switch devices comprise a polarizable material.

15. (Original) The integrated circuit of claim 1 wherein the thin film modifiable conductance switch devices comprise a ferroelectric material.

16. (Original) The integrated circuit of claim 1 wherein the thin film modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage for at least one of two data states.

17. (Original) The integrated circuit of claim 1 embodied in computer readable descriptive form suitable for design, test, or fabrication of the integrated circuit.

18-33 (Canceled)

34. (Currently amended) An integrated circuit comprising a memory array having at least two planes ~~one plane~~ of memory cells formed above a substrate, said memory cells

comprising thin film modifiable conductance switch devices and which cells are arranged in a plurality of series-connected NAND strings, ~~having NAND strings on identical pitch as their respective global bit lines~~ said memory array comprising a first plurality of zias, each of said first plurality of zias respectively coupling a first end of a respective NAND string on each of two or more memory planes to a respective global bit line, and said memory array further comprising a second plurality of zias, each of said second plurality of zias respectively coupling a second end of a respective NAND string on each of two or more memory planes to an associated bias node.

35. (Canceled)

36. (Original) The integrated circuit of claim 34 wherein said switch devices include a charge storage dielectric.

37. (Original) The integrated circuit of claim 36 wherein said charge storage dielectric comprises an oxide-nitride-oxide dielectric stack.

38. (Original) The integrated circuit of claim 34 wherein said switch devices include a floating gate electrode.

39. (Currently amended) The integrated circuit of claim 34 wherein adjacent NAND strings are respectively coupled to a respective global bit line by way of a respective zia structure having a pitch matching that of the ~~adjacent~~ NAND strings.

40. (Original) The integrated circuit of claim 34 further comprising NAND strings including a series select device at each end thereof.

41. (Canceled)

42. (Currently amended) The integrated circuit of claim 34 ~~claim 35~~ wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

43. (Currently amended) The integrated circuit of claim 34 ~~claim 35~~ wherein the substrate comprises a polycrystalline substrate.

44. (Currently amended) The integrated circuit of claim 34 ~~claim 35~~ wherein the substrate comprises an insulating substrate.

45. (Original) The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise silicon nanoparticles.

46. (Original) The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise a polarizable material.

47. (Original) The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise a ferroelectric material.

48. (Original) The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage for at least one of two data states.

49. (Original) The integrated circuit of claim 34 embodied in computer readable descriptive form suitable for design, test, or fabrication of the integrated circuit.

50. (New) The integrated circuit of claim 1 wherein:

wherein half of said NAND strings within the given memory block are each coupled at one end thereof to its respective global bit line, and the other half of said NAND strings within the given memory block are each coupled at the other end thereof to its respective global bit line.

51. (New) The integrated circuit of claim 1 further comprising:

a respective plurality of global bit lines disposed on each of two global bit line layers, said global bit lines having approximately twice the pitch of said NAND strings.

52. (New) The integrated circuit of claim 50 wherein:

each NAND string of a group of M adjacent NAND strings within the given memory block is coupled at one end thereof to its respective global bit line, and each NAND string of an adjacent group of M adjacent NAND strings within the given memory block is coupled at the other end thereof to its respective global bit line.

53. (New) The integrated circuit of claim 52 wherein:

adjacent NAND strings share a single zia coupled to an associated bias node.

54. (New) The integrated circuit of claim 1 further comprising:

a plurality of separate bias nodes, each associated with a respective array block;

wherein NAND strings on two or more memory planes within a given memory block are coupled to a bias node associated with the given memory block.

55. (New) The integrated circuit of claim 54 where the plurality of separate bias nodes comprises a respective bias node for each respective array block.